

**Lithium Ion Battery Application.**  
**Notebook PC , Motor drive Application.**

**Features**

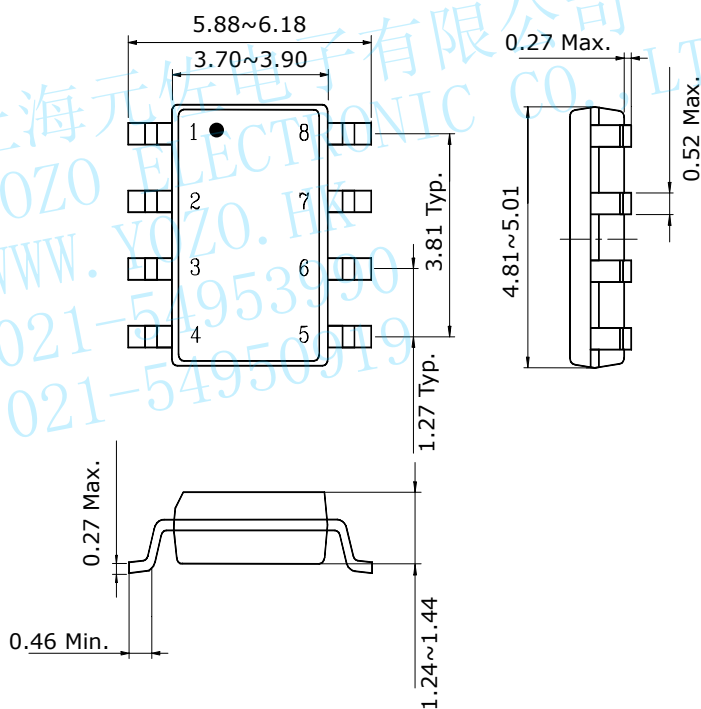
- Low  $C_{RSS}$  :  $C_{RSS}=36pF(Typ.)$
- Low gate charge :  $Q_g=4.2nC(Typ.)$
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=24m\Omega(Typ.)$
- Low  $V_{GS(th)}$  :  $V_{GS(th)}=1.0\sim 3.0V$

**Ordering Information**

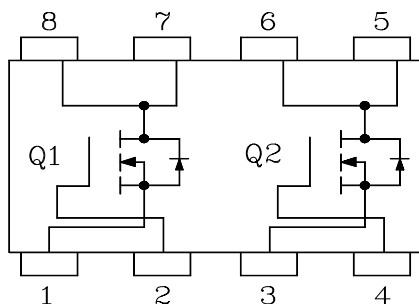
| Type NO. | Marking | Package Code |
|----------|---------|--------------|
| SUF1002  | SUF1002 | SOP-8        |

**Outline Dimensions**

unit : mm



**Block Diagram**



**PIN Connections**

1. Source 1
2. Gate 1
3. Source 2
4. Gate 2
5. Drain 2
6. Drain 2
7. Drain 1
8. Drain 1

**Absolute maximum ratings**

(Ta=25°C)

| Characteristic                   | Symbol    | Rating  | Unit |
|----------------------------------|-----------|---------|------|
| Drain-source voltage             | $V_{DSS}$ | 30      | V    |
| Gate-source voltage              | $V_{GSS}$ | ±20     | V    |
| Drain current (DC)               | $I_D$     | 5.8     | A    |
| Drain current (Pulsed) *         | $I_{DP}$  | 23.2    | A    |
| Total Power dissipation **       | $P_D$     | 2.0     | W    |
| Avalanche current (Single) ②     | $I_{AS}$  | 5.8     | A    |
| Single pulsed avalanche energy ② | $E_{AS}$  | 72      | mJ   |
| Avalanche current (Repetitive) ① | $I_{AR}$  | 5.8     | A    |
| Repetitive avalanche energy ①    | $E_{AR}$  | 3.4     | mJ   |
| Junction temperature             | $T_J$     | 150     | °C   |
| Storage temperature range        | $T_{stg}$ | -55~150 |      |

\* Limited by maximum junction temperature

\* \*\*Device mounted on a glass-epoxy board

| Characteristic     |                  | Symbol        | Typ. | Max | Unit |
|--------------------|------------------|---------------|------|-----|------|
| Thermal resistance | Junction-ambient | $R_{th(J-a)}$ | 62.5 |     | °C/W |

## Electrical Characteristics

(Ta=25°C)

| Characteristic                 | Symbol       | Test Condition                             | Min. | Typ. | Max.      | Unit       |
|--------------------------------|--------------|--------------------------------------------|------|------|-----------|------------|
| Drain-source breakdown voltage | $BV_{DSS}$   | $I_D=250\mu A, V_{GS}=0$                   | 30   | -    | -         | V          |
| Gate threshold voltage         | $V_{GS(th)}$ | $I_D=250\mu A, V_{DS}=V_{GS}$              | 1.0  | -    | 3.0       | V          |
| Drain-source cut-off current   | $I_{DSS}$    | $V_{DS}=30V, V_{GS}=0V$                    | -    | -    | 1         | $\mu A$    |
| Gate leakage current           | $I_{GSS}$    | $V_{DS}=0V, V_{GS}=\pm 20V$                | -    | -    | $\pm 100$ | nA         |
| Drain-source on-resistance     | $R_{DS(on)}$ | $V_{GS}=10V, I_D=2.9A$                     | -    | 24   | 30        | m $\Omega$ |
|                                |              | $V_{GS}=5.0V, I_D=2.9A$                    | -    | 28   | 34        | m $\Omega$ |
| Forward transfer conductance ④ | $g_{fs}$     | $V_{DS}=5V, I_D=5.8A$                      | -    | 12   | -         | S          |
| Input capacitance              | $C_{iss}$    | $V_{GS}=0V, V_{DS}=10V, f=1MHz$            | -    | 370  | 560       | pF         |
| Output capacitance             | $C_{oss}$    |                                            | -    | 60   | 90        |            |
| Reverse transfer capacitance   | $C_{rss}$    |                                            | -    | 36   | 54        |            |
| Turn-on delay time             | $t_{d(on)}$  | $V_{DD}=15V, I_D=5.8A, R_G=10\Omega$<br>③④ | -    | 1.2  | -         | ns         |
| Rise time                      | $t_r$        |                                            | -    | 1.1  | -         |            |
| Turn-off delay time            | $t_{d(off)}$ |                                            | -    | 2.5  | -         |            |
| Fall time                      | $t_f$        |                                            | -    | 1.1  | -         |            |
| Total gate charge              | $Q_g$        | $V_{DS}=15V, V_{GS}=5V, I_D=5.8A$<br>③④    | -    | 4.2  | 6.3       | nC         |
| Gate-source charge             | $Q_{gs}$     |                                            | -    | 0.9  | 1.4       |            |
| Gate-drain charge              | $Q_{gd}$     |                                            | -    | 1.4  | 2.1       |            |

## Source-Drain Diode Ratings and Characteristics

(Ta=25°C)

| Characteristic           | Symbol   | Test Condition                       | Min | Typ | Max | Unit    |
|--------------------------|----------|--------------------------------------|-----|-----|-----|---------|
| Source current           | $I_S$    | Integral reverse diode in the MOSFET | -   | -   | 1.5 | A       |
| Source current(Plused) ① | $I_{SM}$ |                                      | -   | -   | 6.0 |         |
| Forward voltage ④        | $V_{SD}$ | $V_{GS}=0V, I_S=1.5A$                | -   | -   | 1.2 | V       |
| Reverse recovery time    | $t_{rr}$ | $I_S=1.5A, di_s/dt=100A/us$          | -   | 90  | -   | ns      |
| Reverse recovery charge  | $Q_{rr}$ |                                      | -   | 0.5 | -   | $\mu C$ |

Note ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ②  $L=3.4mH, I_{AS}=5.8A, V_{DD}=15V, R_G=25\Omega$
- ③ Pulse Test : Pulse Width < 300us, Duty cycle ≤ 2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

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Fig. 1  $I_D - V_{DS}$

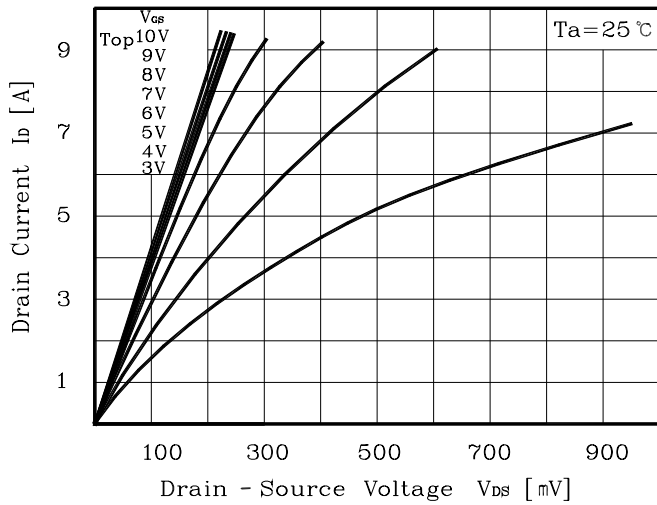


Fig. 2  $I_D - V_{GS}$

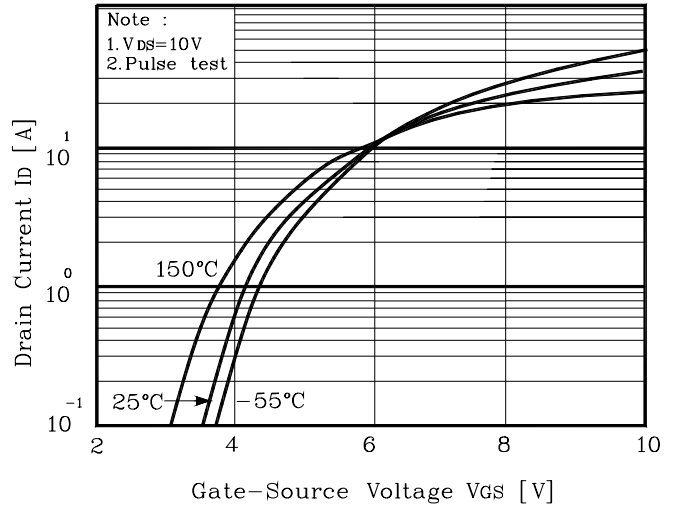


Fig. 3  $R_{DS(on)} - I_D$

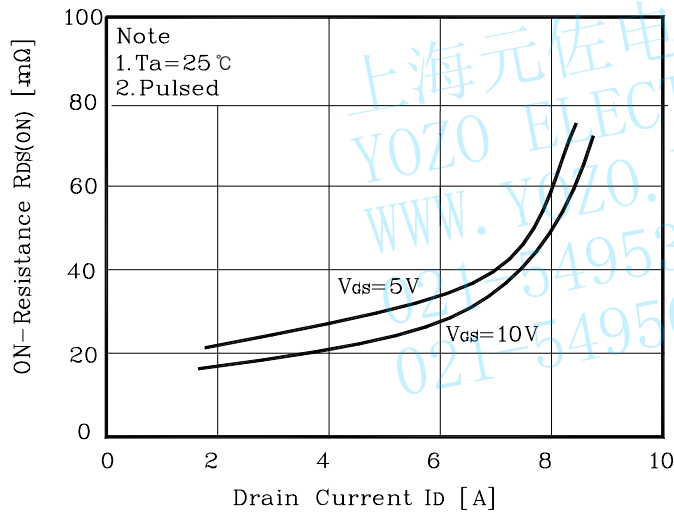


Fig. 4  $I_S - V_{SD}$

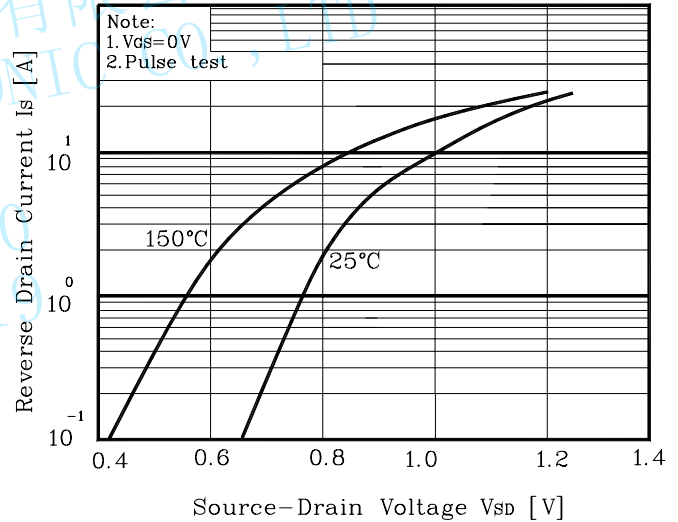


Fig. 5 Capacitance -  $V_{DS}$

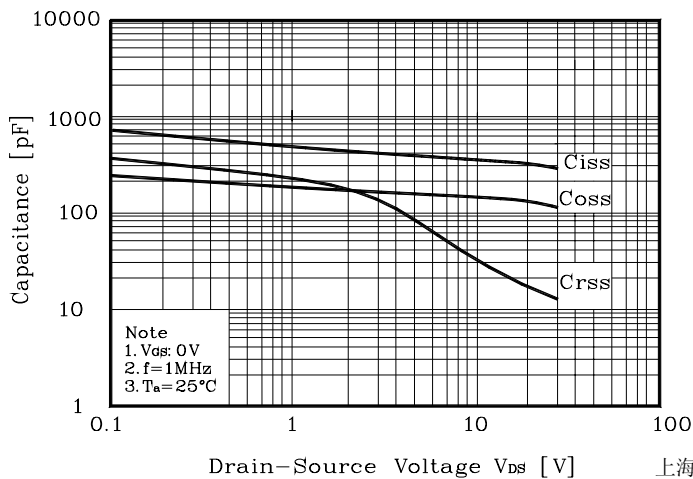
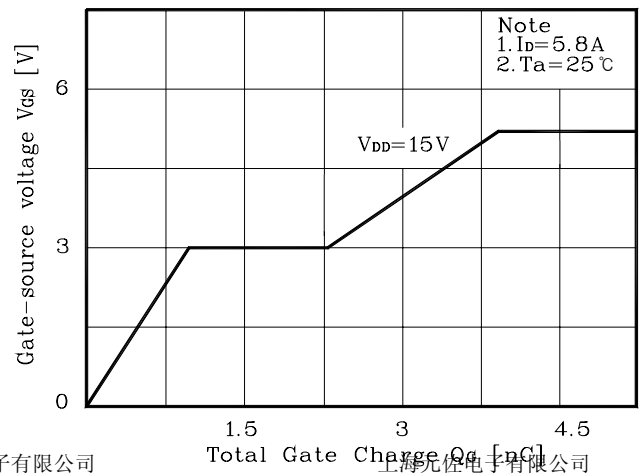
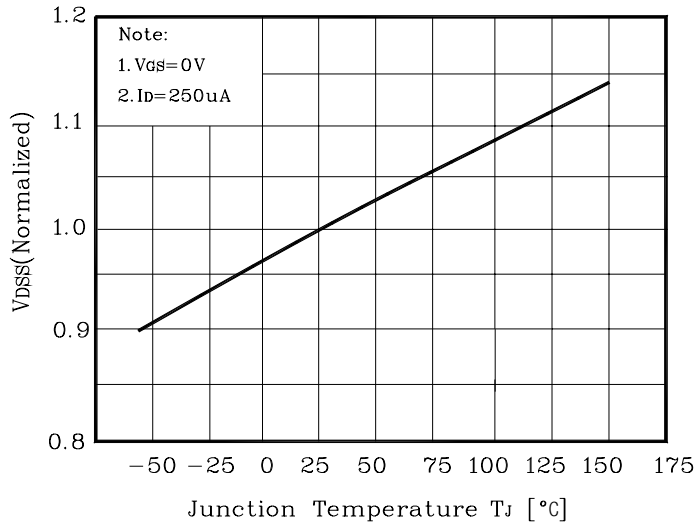


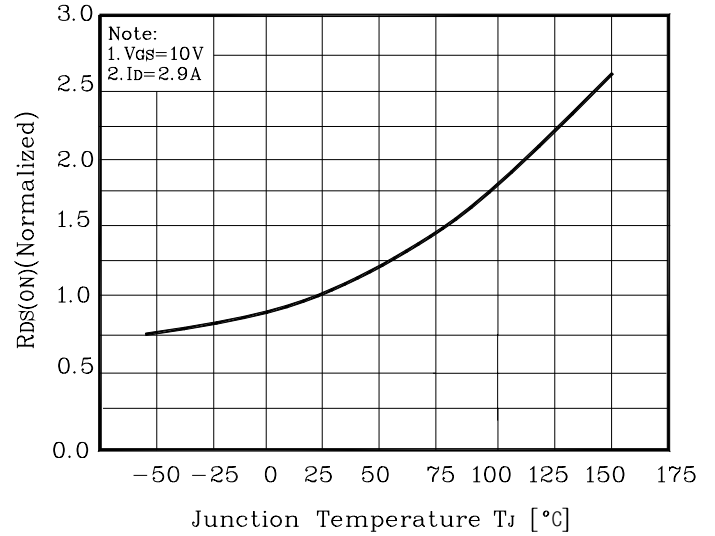
Fig. 6  $V_{GS} - Q_G$



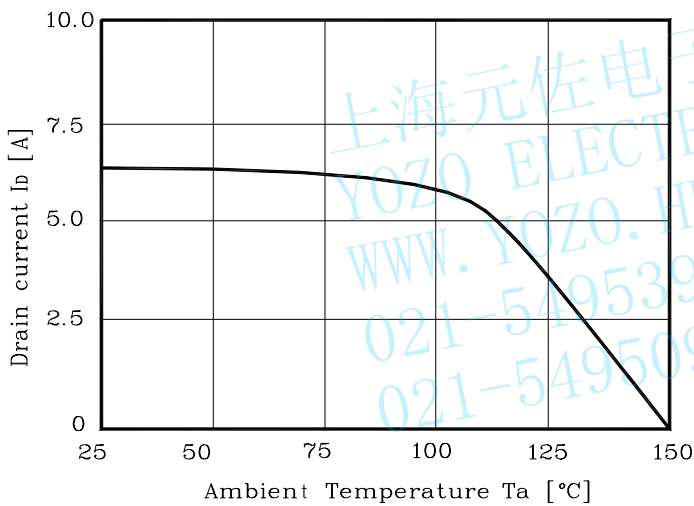
**Fig. 7  $V_{DS} - T_J$**



**Fig. 8  $R_{DS(on)} - T_J$**



**Fig. 9  $I_D - T_a$**



**Fig. 10 Safe Operating Area**

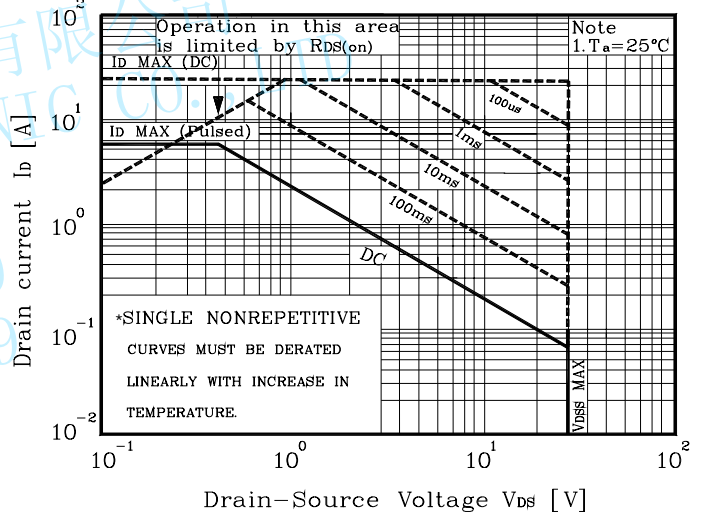


Fig. 11 Gate Charge Test Circuit &amp; Waveform

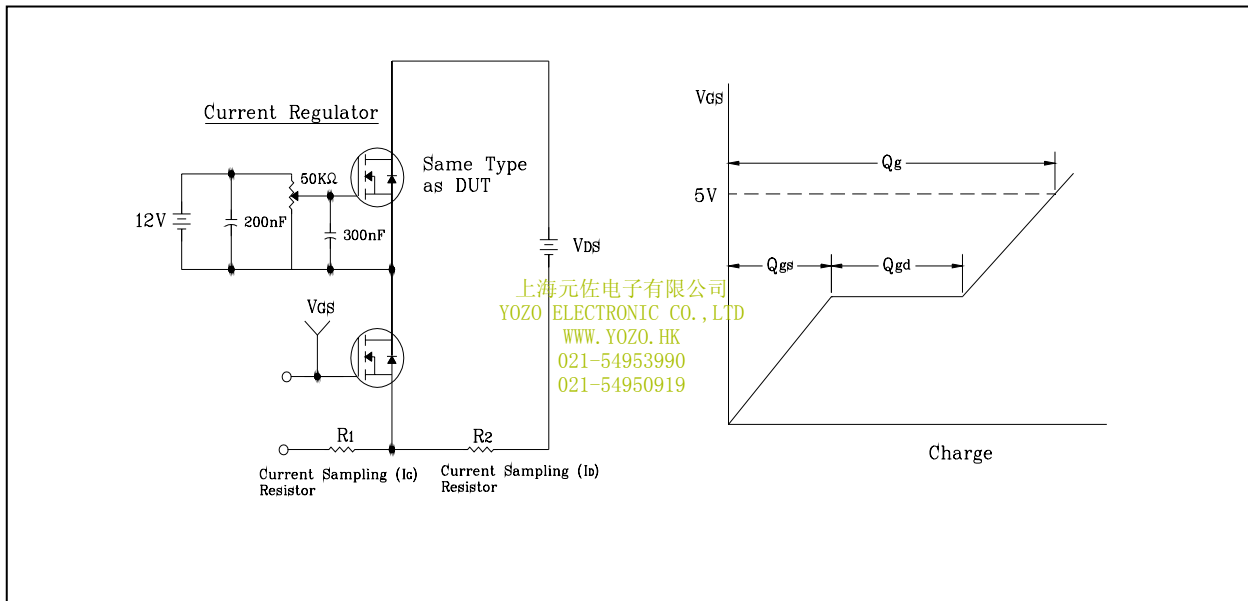


Fig. 12 Resistive Switching Test Circuit &amp; Waveform

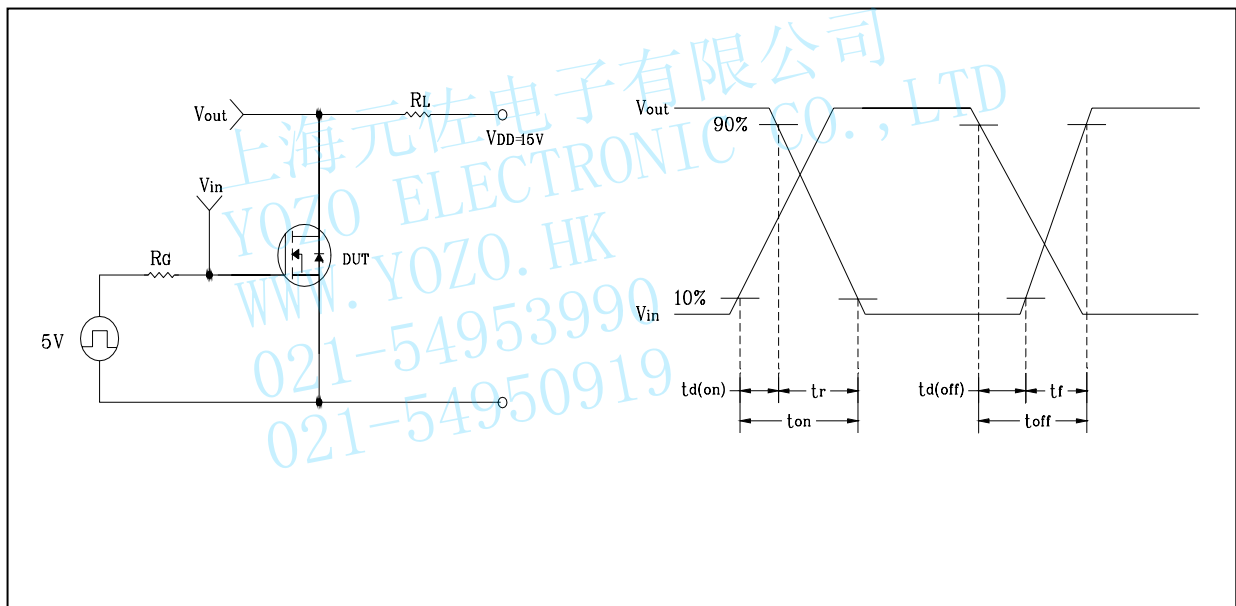
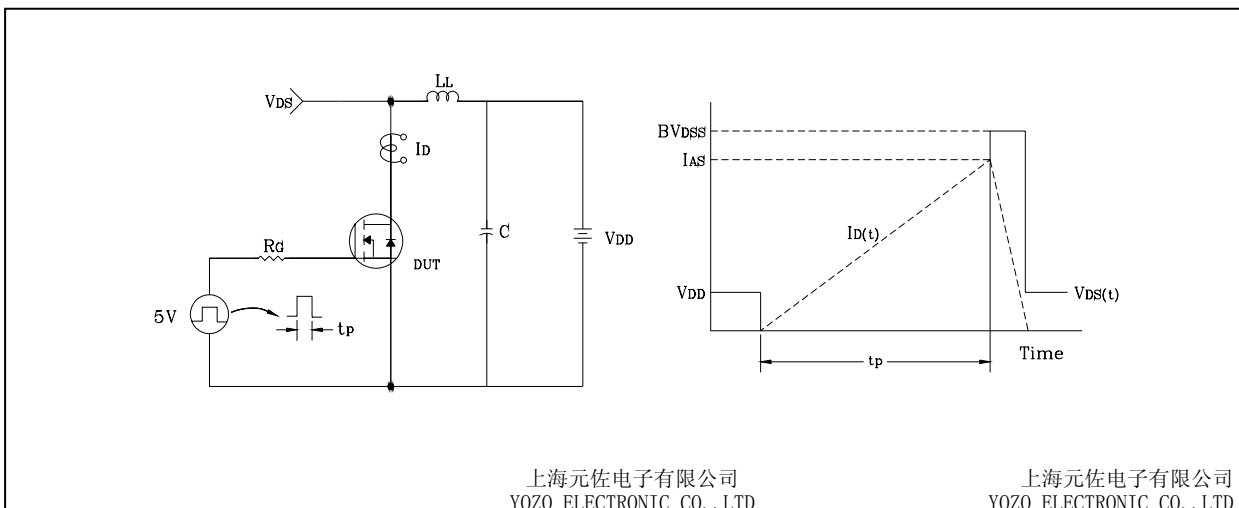
Fig. 13  $E_{AS}$  Test Circuit & Waveform

Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform

