

Description

- High speed switching application.

Features

- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch
- High saturation current capability.

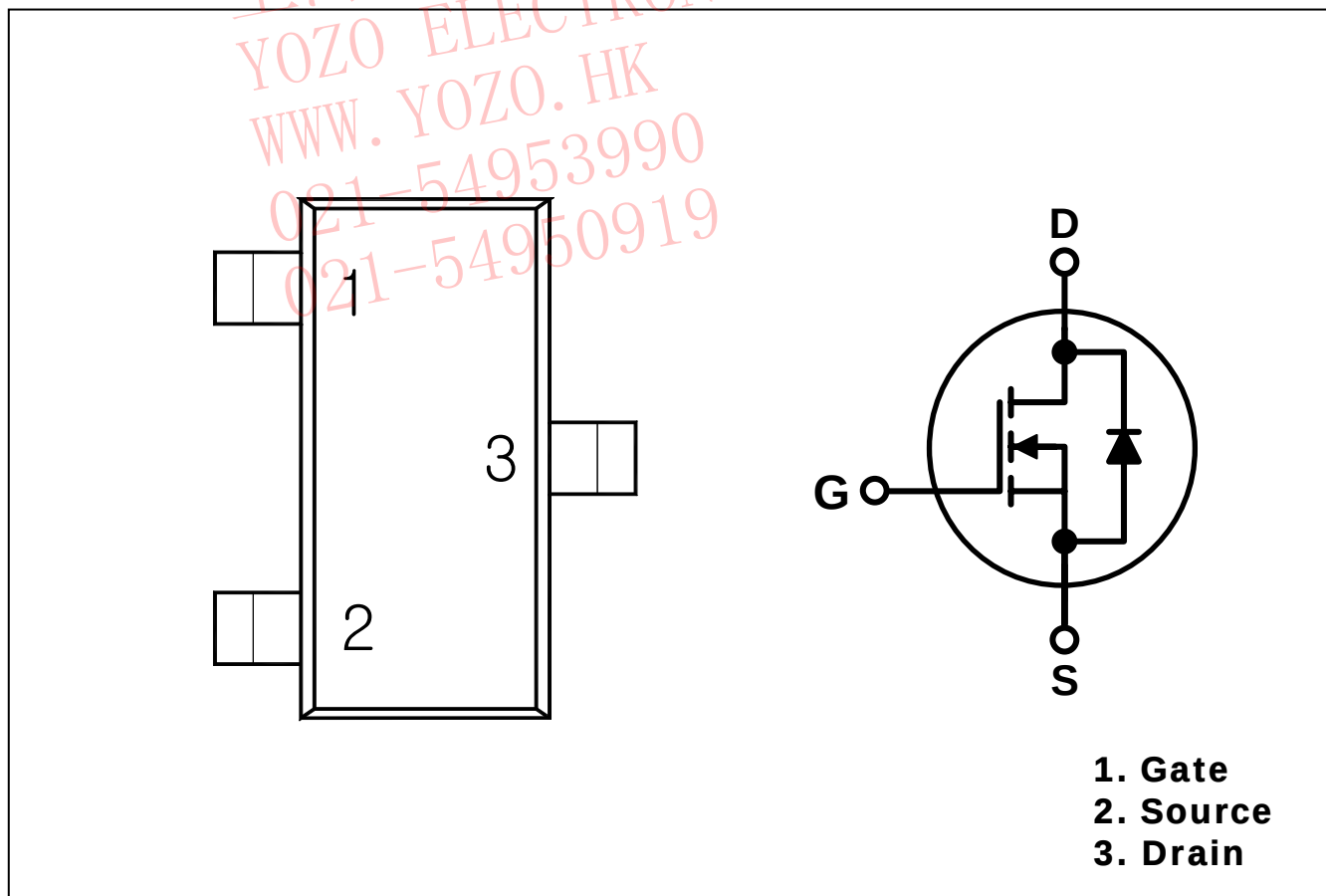
Ordering Information

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Type NO.	Marking	Package Code
STK7002U	K72  ① ②	SOT-323

① Device Code ② Year&Week Code

PIN Connections



Absolute maximum ratings

(Ta=25°C)

Characteristic	Symbol	Ratings	Unit
Drain-Source voltage	V_{DS}	60	V
Gate-Source voltage	V_{GS}	±20	V
Maximum Drain current	I_D	115	mA
Pulsed Drain Current	I_{DP}^*	800	mA
Power Dissipation	P_D	200	mW
Maximum Junction-to-Ambient	R_{thJA}	625	°C/W
Operating Junction and Storage temperature range	T_J, T_{stg}	-55~150	°C

* $PW \leq 10 \mu s$, Duty cycle $\leq 1\%$

Electrical Characteristics

(Ta=25°C)

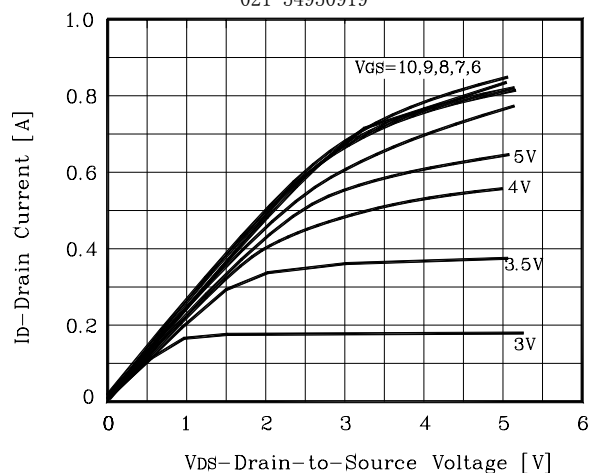
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-Source breakdown voltage	BV_{DS}	$I_D=10\mu A, V_{GS}=0$	60	-	-	V
Gate-Threshold voltage	$V_{GS(th)}$	$I_D=0.25mA, V_{DS}=V_{GS}$	1	2.0	2.5	V
Zero Gate voltage drain current	I_{DSS}	$V_{DS}=60V, V_{GS}=0$	-	-	1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	±100	nA
Drain-Source on-resistance	$R_{DS(ON)}^*$	$V_{GS}=5V, I_D=50mA$	-	3.2	7.5	Ω
		$V_{GS}=10V, I_D=500mA$	-	2.4	7.5	
Forward transconductance	g_{fs}	$V_{DS}=10V, I_D=0.2A$	80	-	-	mS
Input capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0, f=1MHz$	-	22	50	pF
Output capacitance	C_{oss}		-	11	25	
Reverse Transfer capacitance	C_{rss}		-	2	5	
Turn-on time	t_{ON}	$V_{DD}=30V, I_D=0.2A$	-	7	20	ns
Turn-off time	t_{OFF}	$V_{GS}=10V, R_G=25\Omega$	-	11	20	ns

* $PW \leq 300 \mu s$, Duty cycle $\leq 1\%$

Electrical Characteristic Curves

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Fig. 1 $I_D - V_{DS}$



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Fig. 2 $I_D - V_{GS}$

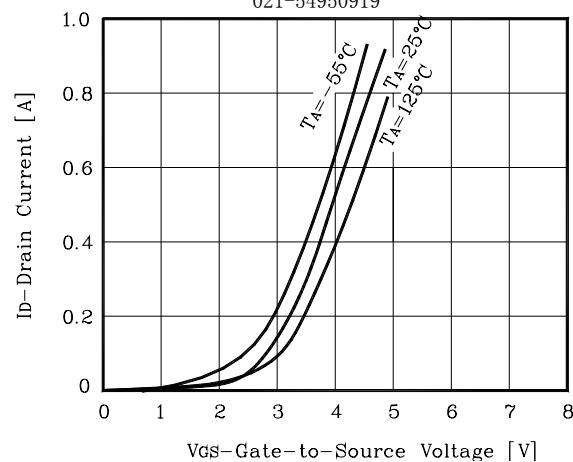


Fig. 3 $R_{DS(on)} - I_D$

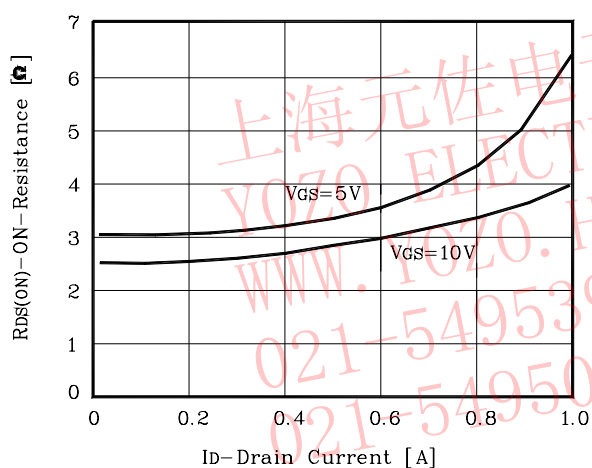


Fig. 4 $C - V_{DS}$

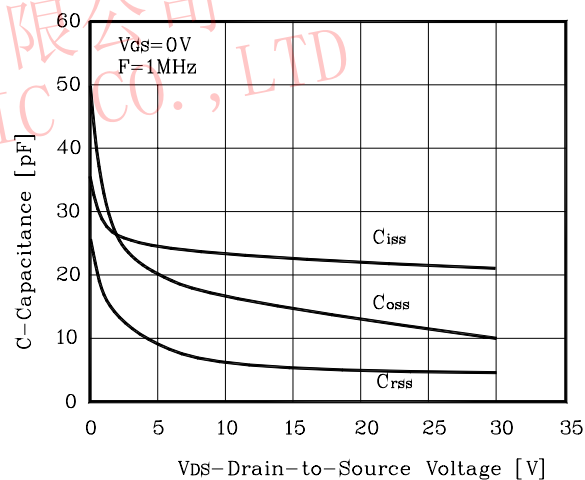


Fig. 5 $V_{GS} - Q_g$

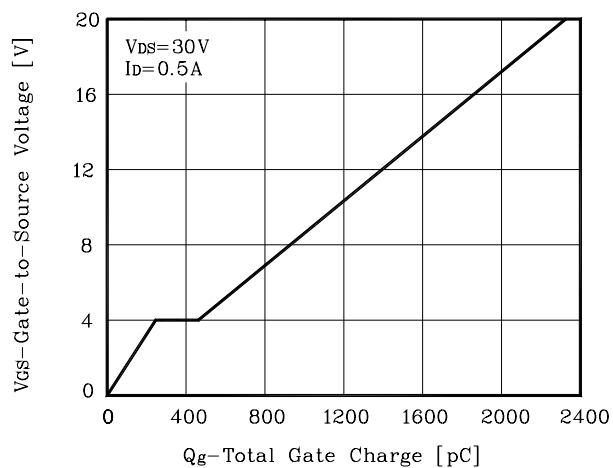
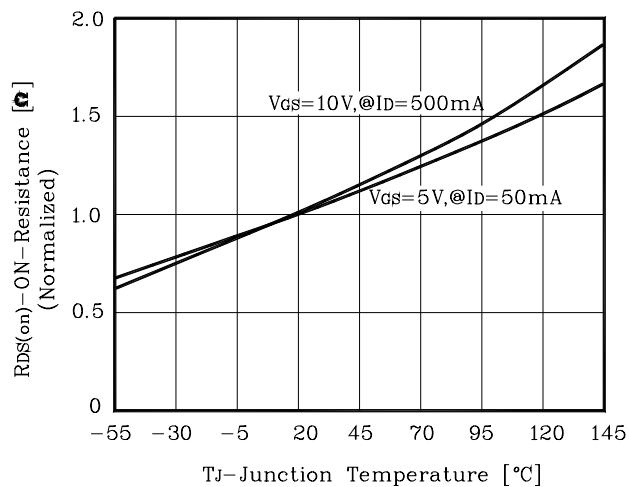


Fig. 6 $R_{DS(on)} - T_J$



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Fig. 7 $R_{DS(on)}$ - V_{GS}

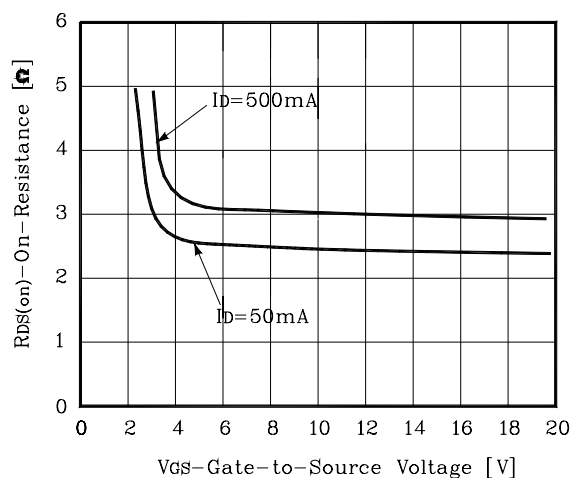


Fig. 8 I_S - V_{SD}

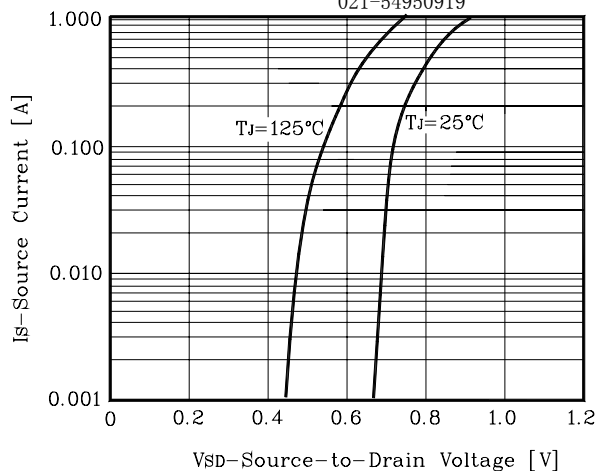


Fig. 9 $V_{GS(th)}$ - T_J

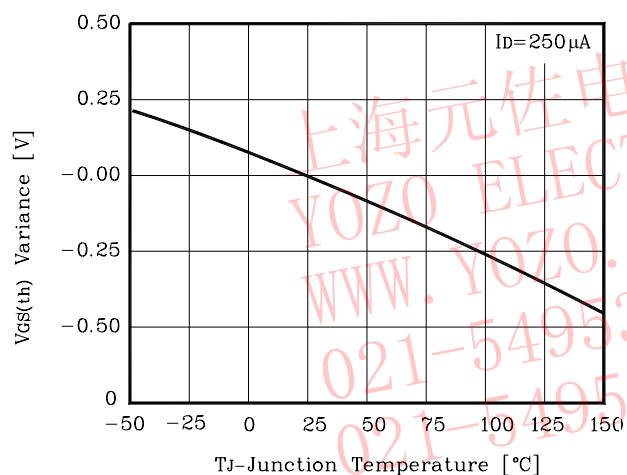


Fig. 10 Safe Operating Area

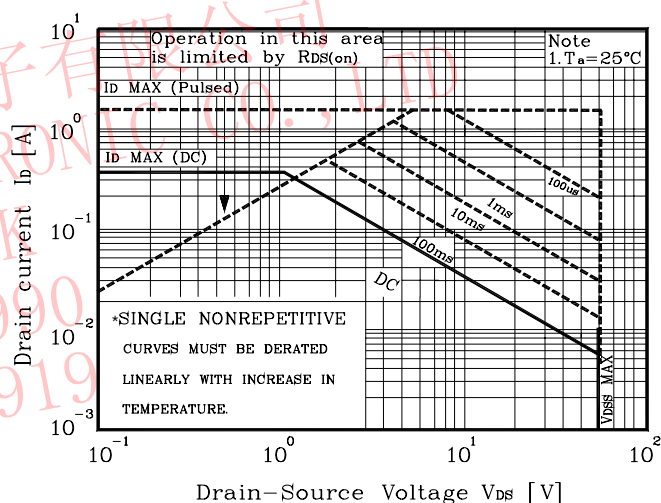


Fig. 11 Gate Charge Test Circuit & Waveform

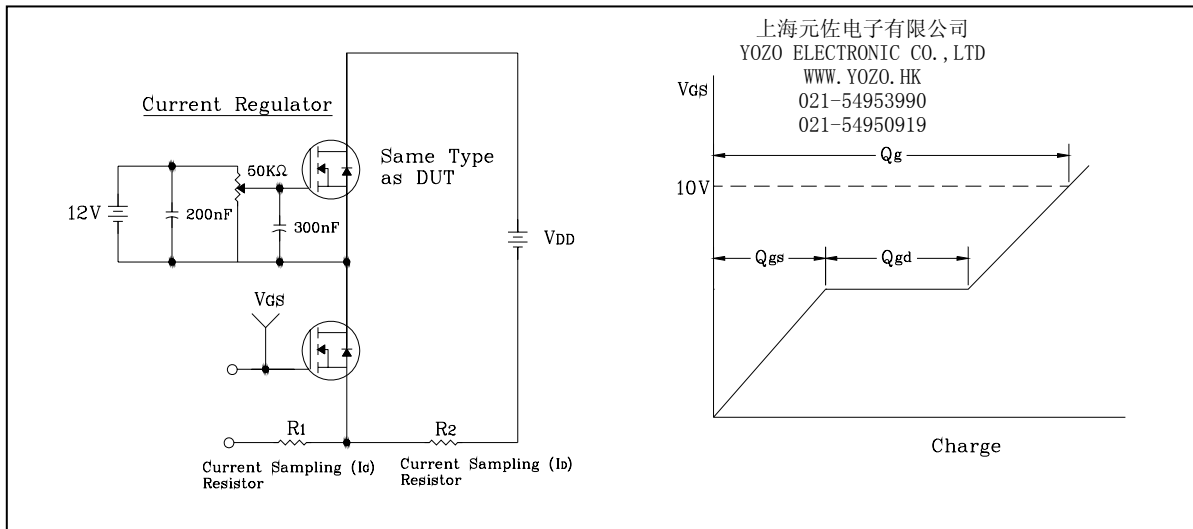


Fig. 12 Resistive Switching Test Circuit & Waveform

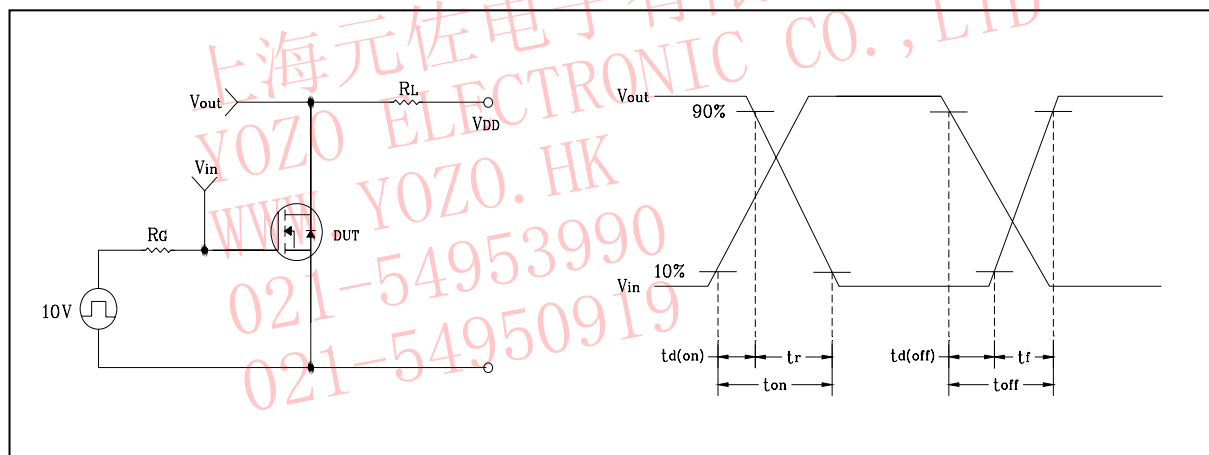


Fig. 13 E_{AS} Test Circuit & Waveform

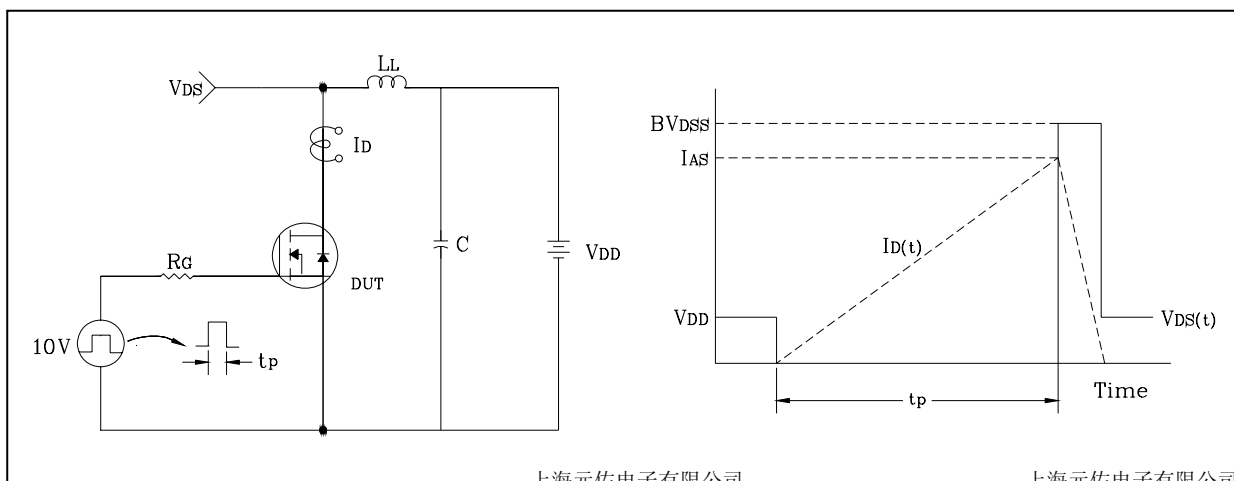
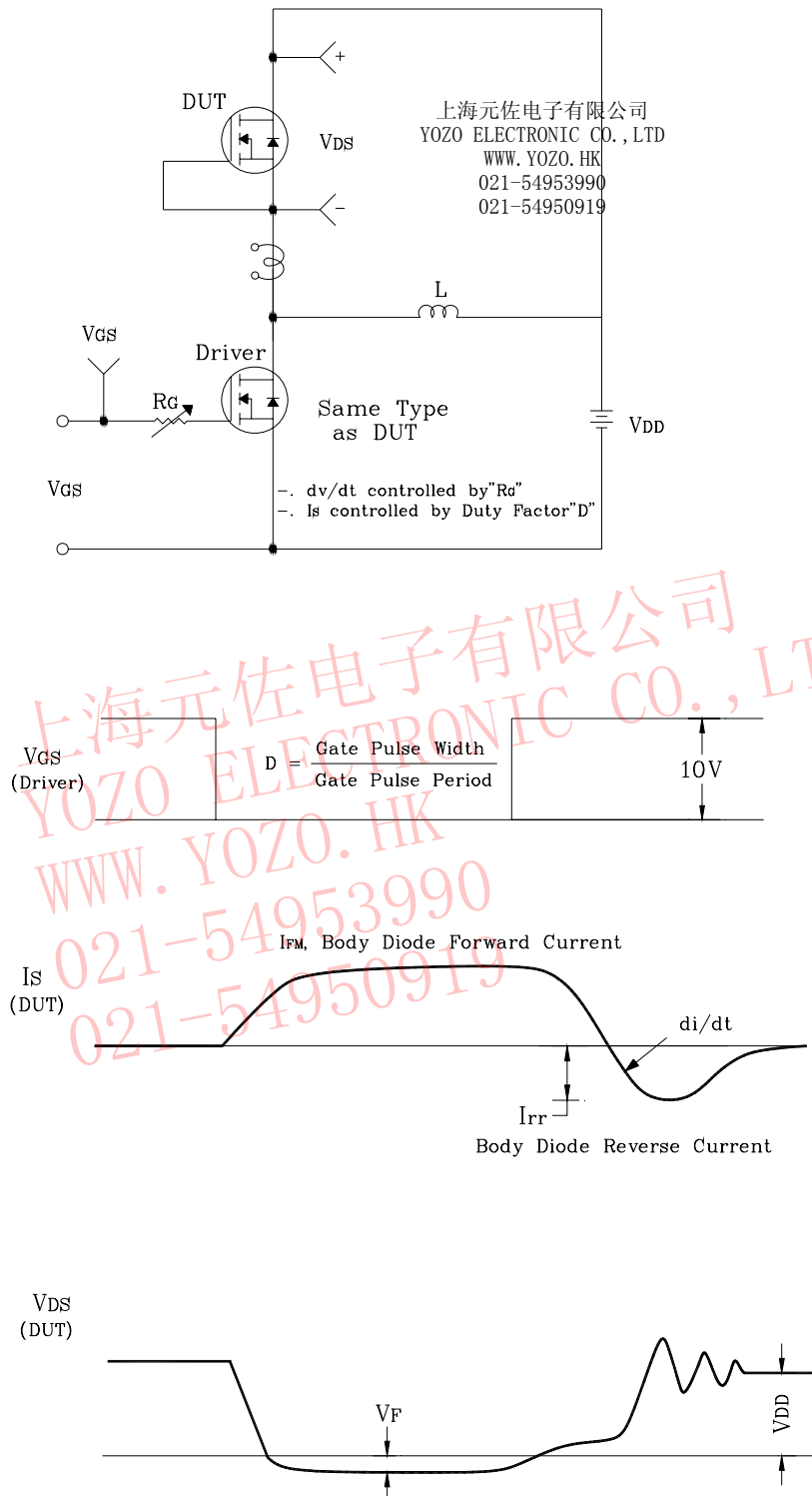
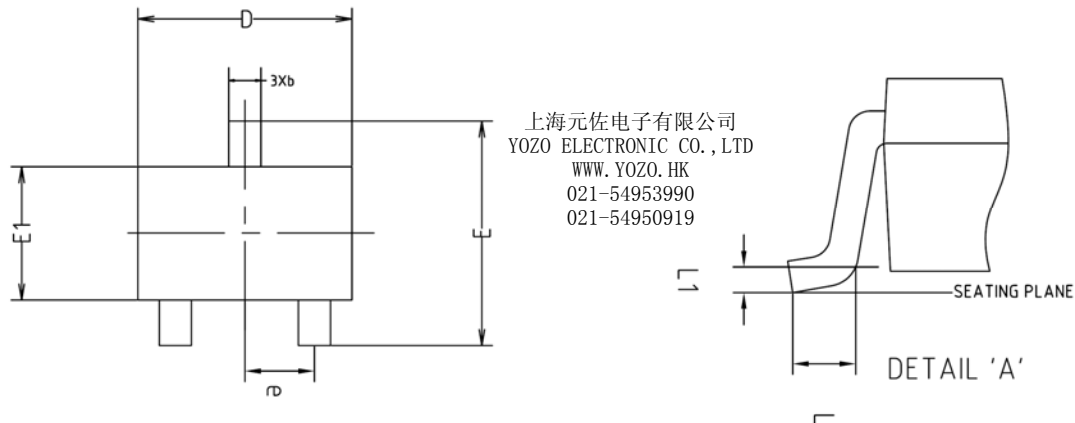


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



Outline Dimension



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.90	-	1.25	
A1	0.00	-	0.10	
A2	0.85	0.90	0.95	
b	0.30	-	0.40	
c	0.10	-	0.25	
D	1.90	2.00	2.10	
E	1.95	2.10	2.25	
E1	1.15	1.25	1.35	
e	0.65BSC			
e1	1.20	-	1.40	
L	0.10	-	-	
L1	0.12BSC			